In the Claims:

1. (Previously Presented) A multi-layer electrode for an integrated circuit, comprising:

a conductive barrier layer;

a first conductive liner disposed over and electrically coupled to the conductive barrier layer;

a second conductive liner disposed over the first conductive liner, the second conductive liner being about 20 to about 50 Angstroms in thickness and being electrically coupled to the first conductive liner and the conductive barrier layer; and

a conductive layer disposed over the second conductive liner, the conductive layer being electrically coupled to the first conductive liner, the conductive barrier layer and the second conductive liner, wherein the conductive layer and the first conductive liner comprise the same material.

2. (Original) The multi-layer electrode according to Claim 1 wherein the second conductive liner comprises a conductive oxide.

3. (Cancelled)

4. (Original) The multi-layer electrode according to Claim 3 wherein the conductive layer and the first conductive liner comprise Pt.

5. (Original) The multi-layer electrode according to Claim 4 wherein the first conductive liner is 200-500 Angstroms thick.

6. (Original) The multi-layer electrode according to Claim 5 wherein the conductive barrier layer comprises TaSiN.

7. (Original) The multi-layer electrode according to Claim 6 wherein the integrated circuit comprises a DRAM or an FRAM.

8. (Previously Presented) A multi-layer electrode for an integrated circuit, comprising:

a conductive barrier layer;

a first conductive liner deposited over and abutting the conductive barrier layer, the first conductive liner comprising a molecular grain structure having a plurality of columns;

a second conductive liner deposited over and abutting the first conductive liner, the second conductive liner comprising a conductive oxide about 20 to about 50 Angstroms in thickness; and

a conductive layer deposited over and abutting the second conductive liner, the conductive layer comprising a molecular grain structure having a plurality of columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner.

9. (Cancelled)

10. (Original) The multi-layer electrode according to Claim 8 wherein the conductive layer and the first conductive liner comprise Pt.

11. (Original) The multi-layer electrode according to Claim 8 wherein the first conductive liner is 200-500 Angstroms thick.

12. (Original) The multi-layer electrode according to Claim 8 wherein the conductive barrier layer comprises TaSiN.

13. (Original) The multi-layer electrode according to Claim 8 wherein the integrated circuit comprises a DRAM or an FRAM.

14. - 20. (Cancelled)

21. (Previously Presented) The multi-layer electrode according to Claim 1 wherein the second conductive liner comprises IrO_2 or RuO_2.

22. (Previously Presented) The multi-layer electrode according to Claim 8 wherein the second conductive liner comprises IrO_2 or RuO_2.

23. (Previously Presented) The multi-layer electrode according to Claim 1 wherein the conductive layer and the first conductive liner comprise Pt, Ir, Ru, Pd, or combinations thereof.

24. (Previously Presented) The multi-layer electrode according to Claim 8 wherein the conductive layer and the first conductive liner comprise Pt, Ir, Ru, Pd, or combinations thereof.

25. (Previously Presented) The multi-layer electrode according to Claim 1, wherein the second conductive liner comprises a thickness such that the second conductive liner is etchable by the same etchant gas used to etch the first conductive liner and the conductive layer.

26. (Previously Presented) The multi-layer electrode according to Claim 1, wherein the conductive layer comprises a molecular grain structure having columns, the conductive layer including a top surface; wherein the first conductive liner comprises a molecular grain structure having columns; wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner; and wherein the second conductive liner prevents diffusion of oxide from the conductive layer top surface through the conductive layer to the conductive barrier layer.

27. (Previously Presented) The multi-layer electrode according to Claim 8, wherein the second conductive liner comprises a thickness such that the second conductive liner is etchable by the same etchant gas used to etch the first conductive liner and the conductive layer.

28. (Previously Presented) An electrode for a semiconductor device, comprising:

a conductive barrier layer;

a platinum liner formed over the conductive barrier layer;

a conductive oxide about 20 to about 50 Angstroms in thickness formed over the platinum liner; and

a platinum layer formed over the conductive oxide, wherein the platinum layer is electrically coupled to the platinum liner.

29. (Previously Presented) The multi-layer electrode according to Claim 28 wherein the conductive oxide comprises IrO_2 or RuO_2.

30. (Cancelled)

31. (Cancelled)

32. (Previously Presented) The electrode of claim 28 wherein the platinum liner has a molecular grain structure having a plurality of columns, wherein the platinum layer has a molecular grain structure having a plurality of columns, and wherein at least one column of the platinum layer is not aligned with the columns of the platinum liner.

33. (Previously Presented) An electrode for a semiconductor device, comprising:

a conductive barrier layer;

a platinum liner formed over the conductive barrier layer;

an iridium oxide liner formed on the platinum liner; and

a platinum layer formed on the iridium oxide liner.